INTERFACING CIRCUIT FOR REDUCING CURRENT CONSUMPTION

Abstract of the Disclosure

An interfacing circuit for reducing current consumption includes a command decoder, an operation controller, and a transmission controller. The command decoder decodes input packet commands and generates corresponding commands. The operation controller generates first through N-th operation signals for performing operations corresponding to the commands in response to a clock signal. The transmission controller transmits the first through N-th operation signals as first through N-th control signals in response to the clock signal. The transmission controller comprises a reset signal generator which generates a reset signal for interrupting the transmission of the first control signal when multiple commands of the first through N-th commands are generated simultaneously, wherein the commands would otherwise incorrectly operate the circuit receiving the first through N-th control signals when the commands are generated simultaneously. In this manner, the interfacing circuit offers the advantage that excessive current does not flow to the memory device, in the event that multiple commands are transmitted simultaneously.

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